## REMARKS

**Applicant's arguments filed February 06, 2002 regarding claims 1-48 have been fully considered but they are not persuasive.**

**Applicant argues that:**

**With respect to claims 1, 13, 26, 30, 36, 42:**

**a) Adiletta does not teach plurality of memory resources. The examiner respectfully disagrees with applicant's position. Adiletta teaches plurality of memory resources that obtain access to a push bus. Adiletta cited that "the six microengines 22a-22f access either the SDRAM or SRAM" [col. 3, lines 43-45; fig. 1, 16a, 16b]. Thus there are more than one memory resource in Adiletta's system.**

**b) Patkar does not disclose "memory resources obtaining access to the push bus based on arbitration by the push bus arbiter. The examiner respectfully disagrees with applicant's position. Patkar clearly teaches memory resources obtaining access to the push bus based on arbitration by the push bus arbiter. Patkar in column 3, lines 44-48 cited "note that each of the arbitrators 32-38 Push and Pull data, instructions, and/or controls signals to and from the global bus 18, with the pushing and/or pulling done in a master role (i.e., active initiation) and the other being done in a slave role (i.e., passive recipient)".**

**2. Claims 1-4, 6-7, 13-14, 16-19, 21, 26-28, 30-31, 34-38, 41-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adiletta 6,606,704, in view of Patkar et al. 6,643,726.**

**Per claim 1:**

**Adiletta teaches a method comprising: identifying memory resources for pushing data to a processing agent; arbitrating use of a push bus by using an arbiter [Fx-cmd bus arbiter, fig. 6-1; col. 3, lines 50-60]; and pushing the data from the memory resources to the processing agent through the push bus, the memory resources obtaining access to the push bus based on arbitration by the bus arbiter [fig. 6-1, 6-2, 6-4; col. 19, lines 42-65; col. 20, lines 1-20]**

**Adiletta does not teach a push bus arbiter using for bus arbitration scheme.**

**Patkar teaches push bus arbiter [col. 3, lines 25-45].**

**It would have been obvious to one having ordinary skill in the art at the time the invention was made to further include the push bus arbiter into Adiletta system. By merely having a dedicate push bus arbiter for the push microengines for handling their own arbitration in a distributed manner, this dedicate arbitration scheme thus eliminates contention for memory as well as contention for a single central arbitrator. This further increase system reliability due to dual arbiter capability [e.g., push bus arbiter for push microengines, and pull bus for pull microengines] so bus arbitration can be processed over two independent data paths, enhancing speed and reliability.**

Applicant thanks the examiner for indicating that he would allow claims 32-35 and 39-41 if rewritten in independent form including all of the limitations of the base claim and any intervening claims. For reasons discussed below, the other claims are also patentable.

According to 35 U.S.C. § 103(c)(1), Adiletta shall not preclude patentability of the applicant's application under 35 U.S.C. § 103. Adiletta was filed on August 31, 1999 and issued on August 12, 2003, and would qualify as prior art to the applicant's application (filed on

January 25, 2002) only under 35 U.S.C. 102(e). At the time the claimed invention of the applicant's application was made, Adiletta and the applicant's application were both owned or subject to an obligation to be assigned to Intel Corporation. Thus, Adiletta is not prior art under 35 U.S.C. § 103.

Patkar does not disclose or suggest "using a push bus arbiter to arbitrate use of a push bus by the memory resources; ... the memory resources obtaining access to the push bus based on arbitration by the push bus arbiter; using a pull bus arbiter to arbitrate use of a pull bus by the memory resources; ... the memory resources obtaining access to the pull bus based on arbitration by the pull bus arbiter," as recited in amended claim 1. The claim amendments are supported by, e.g., page 9, lines 2-5 and 9-12 of the specification.

Patkar discloses a single DRAM 42, and arbiters that push data to or pull data from a global bus 18. Patkar does not disclose or suggest using more than one memory resource. Patkar also does not disclose or suggest an arbiter "to arbitrate use of a push bus by the memory resources" and another arbiter "to arbitrate use of a pull bus by the memory resources," as recited in claim 1.

What is lacking in Patkar is also not disclosed or suggested in Dennin, which discloses context switching when accessing a disk storage device (abstract).

For the reasons above, claim 1 is patentable.

Claims 13 and 26 are patentable for at least similar reasons as claim 1.

The dependent claims are patentable for at least the same reasons as the claims upon which they depend.

Cancelled claims have been cancelled without prejudice. Any circumstance that the applicant has addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner. Any circumstance that the applicant made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims. Any circumstance in which the applicant has amended a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

Enclosed is a $1020.00 check for the Petition for Extension of Time fee. Please apply any other charges or credits to deposit account 06-1050, referencing attorney docket 10559-618001.

Respectfully submitted,

Date: 7/12/2005

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** See attached document certifying that Rex Huang has limited recognition to practice before the U.S. Patent and Trademark Office under 37 CFR § 11.9(b).*

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